

Intel® XScale™ Microarchitecture

Thanks to the Intel® XScale™ microarchitecture, developers of a wide range of Internet applications can optimize the needs of their applications from ultra-low power consumption to high performance processing. Now everything from handheld Internet devices to enterprise Internet infrastructure products can process rich content at all stages of the Internet.

Designed to optimize low power consumption and high performance processing for a wide range of Internet devices from the same processor core.

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This new high-performance, ultra-low power microarchitecture is compliant with the ARM® Version 5TE ISA instruction set (excluding the floating point instruction set). The microarchitecture surrounds the ARM compliant execution core with Instruction and Data Memory Management Units; Instruction, Data and Mini-Data Caches; Write, Fill, Pend and Branch Target Buffers; Power Management, Performance Monitoring, Debug and JTAG Units; Coprocessor Interface; MAC Coprocessor; and Core Memory Bus.

The Intel XScale microarchitecture will be combined with peripherals to provide Applications Specific Standard Products (ASSP) targeted at selected market segments. As an example, the microprocessor core can be integrated with peripherals such as an LCD controller, multi-media controllers and an external memory interface to empower OEMs to develop smaller, more cost-effective handheld devices with long battery life, with the performance to run rich multimedia applications. As another example, the microprocessor core could be surrounded by high-bandwidth PCI interfaces, memory controllers and networking microengines to provide a highly integrated, high performance, I/O or network processor.

The Intel XScale microarchitecture is designed with Intel's state-of-the-art 0.18-micron production semiconductor process technology. This process technology enables the microprocessor core to operate over a wide range of speed and power, producing industry-leading mW/MIPS performance.



Features

Benefits

Intel® Superpipelined RISC Technology	7-stage integer/8-stage memory superpipelined core achieves high speed and ultra-low power
Intel® Dynamic Voltage Management	Dynamic voltage and frequency scaling on-the-fly allows applications to utilize the right blend of performance and power
Intel® Media Processing Technology	Multiply-Accumulate Coprocessor performs two simultaneous 16-bit SIMD multiplies with 40-bit accumulation for efficient media processing
Power Management Unit	gives power savings via idle, sleep, and quick wake-up modes
128-entry Branch Target Buffer	keeps pipeline filled with statistically correct branch choices
32 KB Instruction Cache	keeps local copy of important instructions to enable high performance and low power
32 KB Data Cache	keeps local copy of important data to enable high performance and low power
2 KB Mini-Data Cache	avoids “thrashing” of the D-Cache for frequently changing data streams
32-entry Instruction Memory Management Unit	enables logical-to-physical address translation, access permissions, I-Cache attributes
32-entry Data Memory Management Unit	enables logical-to-physical address translation, access permissions, D-Cache attributes
4-entry Fill and Pend Buffers	promotes Core efficiency by allowing non-blocking and “hit-under-miss” operation with Data Caches
Performance Monitoring Unit	furnishes two 32-bit event counters and one 32-bit cycle counter for analysis of hit rates, etc.
Debug Unit	uses Hardware Breakpoints and 256-entry Trace History Buffer (for flow change messages) to debug programs
32-bit Coprocessor Interface	provides high performance interface between core and coprocessors
64-bit Core Memory Bus with simultaneous 32-bit input path and 32-bit output path	gives up to 4.8 GBytes/sec. @ 600 MHz bandwidth for internal accesses
8-entry Write Buffer	allows the Core to continue execution while data is written to memory

For more information, visit our website at: <http://developer.intel.com/design/xscale/index.htm>



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